AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for simulating hardware circuits during which voltages are calculated at a plurality of circuit nodes, comprising the steps of:

(a) carrying out a first DC-simulation run at the beginning~~begin~~ of a functional cycle,

(b) carrying out a second DC-simulation run at the end of said cycle,

(c) comparing simulated values from both runs at respective circuit nodes, and

(d) storing mismatch information about static error afflicted nodes at which the calculated values differ by more than a predetermined first threshold value.

2. (currently amended) The method according to claim 1 further comprising the steps of:

(e) outputting ~~putting out~~ said mismatch information for a manual correction,

(f) carrying out a transient analysis covering the same functional cycle after correction,

(g) comparing calculated values from said analysis with calculated values from said first or second DC simulation run at respective circuit nodes, and

(h) storing mismatch information about dynamic error afflicted nodes at which the calculated values differ by more than a predetermined second threshold value.

3 - 4. (cancelled)

5. (original) The method according to claim 1 comprising the step of setting the START TIME prior to the begin of a functional cycle.

6. (original) The method according to claim 1 in which the hardware is built according to silicon-on insulator (SOI) technology.

7. (currently amended) A computer system having installed program means comprising program code portions for performing the steps:
   (a) carrying out a first DC-simulation run at the beginning ~~begin~~ of a functional cycle,
   (b) carrying out a second DC-simulation run at the end of said cycle,
   (c) comparing simulated values from both runs at respective circuit nodes, and
   (d) storing mismatch information about static error afflicted nodes at which the calculated values differ by more than a predetermined first threshold value.

8. (currently amended) The computer system according to claim 7 further comprising program code portions for performing the steps:
   (e) outputting ~~putting out~~ said mismatch information for a manual correction,
   (f) carrying out a transient analysis covering the same functional cycle after correction,
   (g) comparing calculated values from said analysis with calculated values from said first or second DC simulation run at respective circuit nodes, and
   (h) storing mismatch information about dynamic error afflicted nodes at which the calculated values differ by more than a predetermined second threshold value.

9 -12. (cancelled)

13. (currently amended) Computer program product stored on a computer-readable ~~usable~~ medium, said product comprising code that, when executed, ~~computer readable program for~~ causes~~ing~~ a computer to perform the method comprising:

(a) carrying out a first DC-simulation run at the beginning ~~begin~~ of a functional cycle,

(b) carrying out a second DC-simulation run at the end of said cycle,

(c) comparing simulated values from both runs at respective circuit nodes, and

(d) storing mismatch information about static error afflicted nodes at which the calculated values differ by more than a predetermined first threshold value.

14. (currently amended) The computer program product according to claim 13 wherein said method further comprises performing the steps:

(e) outputting ~~putting out~~ said mismatch information for a manual correction,

(f) carrying out a transient analysis covering the same functional cycle after correction,

(g) comparing calculated values from said analysis with calculated values from said first or second DC simulation run at respective circuit nodes, and

(h) storing mismatch information about dynamic error afflicted nodes at which the calculated values differ by more than a predetermined second threshold value.